**Claims**

What is claimed is:

1. A method of operating an electronic device having a plurality of memory devices, each memory device having at least two sub-arrays therein, the method comprising:

individually addressing each sub-array of each said memory device by communicating an address specific to that sub-array across an address bus coupled to all said memory devices, and by individually selecting said individual memory device from among said plurality of memory devices.

2. The method of claim 1, wherein said plurality of memory devices are formed as a part of a memory module.

3. The memory device of claim 1, wherein said electronic device comprises a computer.

4. A method of operating an electronic device having a plurality of memory devices associated therewith, each memory device having at least two sub-arrays therein, the method comprising:

individually selecting at least one individual memory device from among said plurality of memory devices; and

individually addressing a selected sub-array of said selected memory device by communicating an address specific to that sub-array across an address bus coupled to each memory device of said plurality of memory devices to access a memory cell in said selected sub-array.

5. The method of claim 4, further comprising maintaining at least one memory device of said plurality of devices in a standby mode, while accessing said memory cell in said selected sub-array.

6. The method of claim 4, wherein said individual selection of said at least one individual memory device comprises decoding a plurality of activation signals to determine the memory device to be individually selected.

7. The method of claim 4, further comprising:

selecting a number of said memory devices from said plurality of memory devices; and

accessing a number of data bits, wherein said number of data bits accessed is greater than said number of memory devices selected.

8. A method of configuring an electronic system having a plurality of memory devices therein, comprising:

providing a plurality of memory devices, each memory device having a plurality of banks therein;

coupling a plurality of data lines to each memory device, with each data line coupled to only one bank in each memory device;

coupling an address bus to each memory device, said address bus configured to allow access of a memory cell in any bank of said plurality of banks in each said memory device; and

providing at least one chip select mechanism to facilitate individual selection of each memory device, said system configured to allow fewer than all of said plurality of memory devices to be selected and activated, while the remaining memory devices of said plurality of memory devices are unselected and in a low power mode.

9. The method of claim 8 wherein said memory devices are physically coupled to a memory module.

10. The method of claim 8 wherein said electronic system comprises a computer.